In the Claims

1. **(As Filed)** During the testing of the operation of processing unit, a system for identifying the occurrence of a processor unit debug halt condition, the system comprising:

timing trace apparatus responsive to signals from the processor unit, the timing trace apparatus generating a timing trace stream;

program counter trace apparatus responsive to signals from the processing unit, the program counter trace apparatus generating a program counter trace stream; and

synchronization apparatus applying periodic signals to the timing trace apparatus and to the program counter trace apparatus, the periodic signals providing a synchronization between trace streams;

wherein the program counter trace apparatus is responsive to a debug halt signal, the program counter trace apparatus generating marker signal group identifying the occurrence of the debug halt signal and relating the debug halt signal to the timing trace stream.

2. **(As Filed)** The system as recited in claim 1 wherein the marker signal group includes a program counter address, a timing index and a periodic sync ID.

3. **(As Filed)** The system as recited in claim 1 further comprising:

data trace apparatus responsive to signals from the processing unit, the data trace apparatus generating a data trace stream, wherein the periodic signals are applied to the data trace apparatus; and

a host processing unit, the host processing unit responsive to the timing trace stream, the program counter trace stream and the data trace stream, the host processing unit reconstruction the processing activity of the processing unit from the trace streams.

4. **(As Filed)** The method for communicating an occurrence of a debug halt signal from a target processor unit to a host processing unit, the method comprising:

generating a timing trace stream, a program counter trace stream, and data trace stream, and

in the program counter trace stream, including a marker signal group indicating an occurrence of debug halt signal and relating the occurrence of the debug halt signal to the data trace stream and to the timing trace stream.

5. **(As Filed)** The method as recited in claim 4 further comprising:

in the marker signal group, including a periodic sync ID, a timing index and a program counter address.

6. **(Allowed)** In a processing unit test environment wherein a target processor transmits a plurality of trace streams to a host processing unit, a marker signal group

included in a trace signal stream, the marker signal group comprising:

indicia of the occurrence of a debug halt signal;

indicia of the relationship of the occurrence of the debug halt signal to the target processor clock; and

indicia of the relationship of the occurrence of the debug halt signal to the target processor program execution.

Please amend Claim 7 as follows.

7. **(Currently Amended)** In a target processing unit generating trace test signals for transfer to a host processing unit, program counter trace generation apparatus comprising:

a storage unit;

a decoder unit responsive to a ~~rest~~ reset signal for storing a signal group identifying the debug halt signal in the storage unit in a first location in the storage unit, the decoder unit generating a control signal;

a gate unit responsive to the control signal, the gate unit transmitting processor signals applied thereto to the storage unit for storage at defined locations, the signals stored in the storage unit forming a debug halt sync marker; and

a FIFO unit coupled to the storage unit, the FIFO unit receiving the debug halt sync marker when the debug halt

sync marker is complete, the FIFO unit transferring the debug halt sync marker to the host processing unit.

Please cancel Claim 8 as follows.

8. **(Currently Cancelled)** The program counter trace apparatus as recited in claim 7 responsive to a selected control signal for transferring debug halt sync marker in the FIFO unit to an output port of the target processor.

Please amend Claim 9 as follows.

9. **(Currently Amended)** The program counter trace apparatus as recited in claim 10 wherein the debug halt sync marker signal includes a plurality of packets.

Please amend Claim 10 as follows.

10. **(Currently Amended)** The program counter trace apparatus as recited in claim 10 wherein the processor signals applied to the gate unit include a program counter address, a periodic sync ID, and a timing index.